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1 Integrated architectural/physical planning approach for minimization of current surge in high performance clock-gated microprocessors
Yiran Chen, Kaushik Roy, Cheng-Kok Koh
August 2003 **ISLPED '03:** Proceedings of the 2003 international symposium on Low power electronics and design
Publisher: ACM Request Permissions
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We propose an integrated architectural/physical planning approach to reduce the power supply noise due to current surge in high performance, general-purpose, clock-gated microprocessors. The proposed approach combines dynamic selection of functional ...

Keywords: inductive noise, power supply noise

2 Theoretical and practical aspects of Iddq Settling: impact on measurement timing and quality
B. Straka, H. Manhaeve, J. Brenkuš, S. Kerckenaere
March 2008 **DATE '08:** Proceedings of the conference on Design, automation and test in Europe
Publisher: ACM
Full text available: Pdf (489.89 KB) Additional Information: full citation, abstract, references, index terms

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This paper discusses the parameters involved in making fast and reliable quiescent current (Iddq or Issq) measurements, with particular attention to the test setup and the point of measurement. For that purpose a detailed theoretical and practical study ...

3 Priority assignment optimization for minimization of current surge in high performance power efficient clock-gated microprocessor
Yiran Chen, Kaushik Roy, Cheng-Kok Koh
January 2004 **ASP-DAC '04:** Proceedings of the 2004 Asia and South Pacific Design Automation Conference
Publisher: IEEE Press
Full text available: Pdf (272.86 KB) Additional Information: full citation, abstract, references

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We propose an integrated architectural/physical-planning approach named priority assignment optimization to minimize the current surge in high performance power efficient clock-gated microprocessors. The proposec approach balances the current demands ...

4 Self-biased high-bandwidth low-jitter 1-to-4096 multiplier clock generator PLL
John G. Maneatis, Jaeha Kim, Iain McClatchie, Jay Maxey, Manjusha Shankaradas
June 2003 **DAC '03:** Proceedings of the 40th annual Design Automation Conference
Publisher: ACM Request Permissions
Full text available: Pdf (490.09 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 13, Downloads (Overall): 320, Citation Count: 0

A self-biased PLL uses a sampled feed-forward filter network and a multi-stage inverse-linear programmable current mirror for constant loop dynamics that scale with reference frequency and are independent of multiplication factor, output frequency, and ...

Keywords: PLL, adaptive bandwidth, analog circuits, clock generation, clock multiplication, frequency synthesis, phase-locked loop, self biased